Amendments to the Specification

Please replace the paragraph beginning on page 8, line 2 with the following amended paragraph:

The sense amplifiers 140-00 to 140mn have input thereto a voltage of the bit lines BL and BLb when a level of the control line SAE0 to SAEk are high, and compare these voltages. Then, the sense amplifier supplies a high level to the bit line which has a higher voltage and supplies a low level to the bit line which has a lower voltage. Also, the sense amplifiers output the high level and the low level to the digit lines DB and DBb through the gate transistors GT and GTb.

Please replace the paragraph beginning on page 10, line 4 with the following amended paragraph:

The array control circuit 200 turns the plate line PL0 and the judgement plate line JPL0 to the low level at t4 [[t3]]. When the plate line PL0 becomes the low level and the bit line BL and the plate line PL0 become the same voltage level, the writing operation to the ferroelectric capacitor C0 is completed. Also, since the bit line BL and the judgement plate line JPL0 become the same voltage level, the writing operation to the ferroelectric capacitor JC0 is completed. Since there is a voltage between the bit line BLb and the judgement plate line JPL0, the "1" value is rewritten in the ferroelectric capacitor JC1.

Please replace the paragraph beginning on page 12, line 5 with the following amended paragraph:

The array control circuit 20 turns the word line WL0 and the judgement word lines [[WL0]] JWL0 and JWL1 to the low level at t12. As a result, all the writing operation to the judgement ferroelectric capacitors JC0 and JC1 is completed.

Please replace the paragraph beginning on page 18, line 21 with the following amended paragraph:

The plate line driver 813 includes AND gates 931-0 to 931-n, an OR gate 932 and inverters 933-1 to 933-j as shown in Fig. 9(C). The AND gates 931-0 to 931-n input an output signal of the OR gate 932, the row addresses AX1 to AXj and the inverted signal of the row addresses AX1 to AXj. The OR gate [[922]] 932 outputs a logical OR of a plate line enable signal PLEN and a test mode signal TM4. The inverters 933-1 to 933-j invert the row addresses AX1 to AXj. In the plate line driver 813, when the plate line enable signal PLEN or the test mode signal TM4 is turned to the high level, one of the plate line PL0 to PLm is turned to the high level in response to the row addresses AX1 to AXj.

Please replace the paragraph beginning on page 19, line 17 with the following amended paragraph:

The judgement plate line driver 815 includes AND gates 951-0 to 951-3 and

inverters 952-0 and 952-1. The [[and]] AND gates 951-0 to 951-3 have input thereto a test mode signal TM6, ~~a test mode signal TM6~~[[,]] the test mode signals TM7 and TM8 and the inverted signal of the test mode signals TM7 and TM8. The inverters 952-0 and 952-1 invert the test mode signals TM7 and TM8. In the judgement plate line driver 815, when the test mode signal TM6 is turned to the high level, one of the judgement plate ~~line JWL0 to JWL3~~ lines JPL0 to JPL3 is turned to the high level in response to the level of the test mode signals TM7 and TM8.

Please replace the paragraph beginning on page 20, line 15 with the following amended paragraph:

The control logic circuit 830 generates a data control signal DATACON and each of enable signals VREFEN, WLEN, PLEN, YSELEN and BLKEN in response to the test mode signal TM2 and the input signal.